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EXAMINER	
DOLE, TIMOTHY J	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/829,749	Applicant(s) EDDY ET AL.	
	Examiner Timothy J. Dole	Art Unit 2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-7,9-14 and 16-22* is/are rejected.

7)☒ Claim(s) *2,8 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morrison et al. in view of Leedy (USPN 6,288,561).

Referring to claim 1, Morrison et al. discloses an electronic circuit test and repair apparatus comprising: at least one wiring analyzer (fig. 3 (12)) to locate shorts between conductors (column 6, lines 1-4), said conductors being on a surface of or embedded in a carrier substrate (column 4, lines 23-31), said conductors being intended to interconnect components to be mounted on said carrier substrate to form a circuit, said carrier substrate being devoid of all said components (column 4, lines 20-23); and a cluster probe (column 4, lines 35-36) to contact said conductors in a manner controlled by said wiring analyzer (column 4, lines 41-51).

Morrison et al. does not disclose a current source to provide a current sufficient to remove shorts.

Leedy discloses a current source to provide current sufficient to remove shorts (column 6, lines 60-64). It should be noted, Leedy discloses that "high voltage or current" (column 6, line 62) is used in the repair process. Leedy also states that for repairing

circuits, the computer can supply appropriate control signals so that "appropriate voltage or current can be applied between the probe points" (column 7, lines 64-67).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the current source of Leedy into the apparatus of Morrison et al. for the purpose reducing the number of steps and therefore time needed to produce functional boards that are free of defects (column 2, lines 4-9).

Referring to claim 3, Morrison et al. as modified discloses the apparatus as claimed except for a controller for automatic positioning of said cluster probe.

Leedy discloses a controller for automatic positioning of the cluster probe (claim 21).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Morrison et al. for the purpose of automatically positioning the cluster probe to reduce the possibility of human error or further damage due to additional handling.

Referring to claim 5, Morrison et al. discloses the test and repair apparatus as claimed except for a controller having voltage stress test capability.

Leedy et al. discloses a controller having voltage stress test capability. It should be noted, Leedy states that a computer can provide control signals to the probes so that high voltage can be provided between the appropriate probe points (column 6, lines 60-63), which could be considered a controller for voltage stress testing.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Morrison et al. for

the purpose of having voltage stress test capability, since it is useful in testing, to make sure a repaired short does not regenerate and to avoid further faults.

Referring to claim 6, Morrison et al. discloses the apparatus as claimed except for a controller to automate at least one of said locating of circuit shorts and said removing of said located circuit shorts.

Leedy discloses a controller to automate at least one of said locating of circuit shorts and said removing of said located circuit shorts (claim 6 (b) and (d)).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Morrison et al. for the same purpose as given in claim 3, above.

Referring to claim 7, Morrison et al. discloses the apparatus as claimed wherein said at least one wiring analyzer additionally locates open circuits (column 6, lines 1-4) that are defects in said carrier substrate (column 1, lines 22-32).

3. Claims 14 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. in view of Leedy.

Referring to claim 14, Lo et al. discloses an apparatus for test and repair of wiring interconnect packages, comprising: at least one wiring analyzer (fig. 1 (40)) to locate circuit shorts, a current source (fig. 1 (30)), and a cluster probe (column 4, lines 39-41) to contact predetermined locations on a wiring interconnect package under evaluation. It should be noted that a cluster probe comprises a set of test probes that all simultaneously contact the device under test. Therefore, according to column 1, lines 17-19, the probing device as disclosed by Lo et al. could be called a cluster probe.

Lo et al. does not disclose that the test and repair apparatus is able to provide a current sufficient to remove shorts.

Leedy discloses a current source to provide current sufficient to remove shorts (column 6, lines 60-64).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the current source of Leedy in the apparatus of Lo et al. for the purpose of removing shorts and repairing electronic circuits (column 6, lines 55-60).

Referring to claim 16, Lo et al. as modified discloses the apparatus as claimed except for a controller to automatically position the cluster probe.

Leedy discloses a controller for automatic positioning the cluster probe (claim 21).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Lo et al. for the same purpose as given in claim 3, above.

Referring to claim 17, Lo et al. discloses the test and repair apparatus as claimed except for a controller having voltage stress test capability.

Leedy et al. discloses a controller having voltage stress test capability. It should be noted that the computer disclosed by Leedy could be considered a controller for voltage stress testing as shown in claim 5, above.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Lo et al. for the same purpose as given in claim 5, above.

Referring to claim 18, Lo et al. discloses the apparatus as claimed except for a controller so that at least one of locating circuit shorts and removing circuit shorts is animated.

Leedy discloses a controller to automate at least one of locating circuit shorts and removing circuit shorts (claim 6 (b) and (d)).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Lo et al. for the same purpose as given in claim 3, above.

4. Claims 9-13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. in view of Leedy (USPN 6,288,561), and further in view of Kerschner.

Referring to claim 9, Lo et al. discloses a method of testing wiring interconnect packages comprising: contacting a predetermined set of locations on a wiring interconnect package using a cluster probe containing a plurality of probes (claim 1); applying a predetermined set of voltages in a predetermined sequence to predetermined probes in the cluster probe (claim 1); and measuring a response to each application of voltages to detect any short circuits in the wiring interconnect package (claim 1).

Lo et al. does not disclose that open circuits will be detected, or that for any detected short circuits, a predetermined voltage will be applied to attempt to remove the detected short circuits, where the applying of voltages to attempt to remove a detected short circuit and measuring of responses to detect any short circuits uses the same apparatus that would be used for attempting to remove the short circuits.

Kerschner discloses a method to detect open circuits (column 4, lines 19-39).

Leedy discloses a test and repair method where for any detected short circuits, a predetermined voltage is applied to attempt to remove the detected short circuits (column 6, lines 55-58), where the applying of voltages to attempt to remove a detected short circuit and measuring of responses to detect any short circuits uses the same apparatus that is used for attempting to remove the short circuits (column 7, lines 10-15).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the method of open circuit detection of Kerschner and the repair method of Leedy into the method of Lo et al. for the purpose of detecting open circuits, since further fault detection is useful in determining the quality of a device under test, and repairing short circuits since it is stated by Lo et al. that "it is desirable to determine which networks are shorted together, so that the circuit can be repaired" (column 6, lines 54-56).

Referring to claim 10, Lo et al. discloses the method as claimed except for automating one of the following: the contacting at a predetermined set of locations; the detecting of abnormal open and short circuits; and the attempting to remove the short circuits.

Leedy discloses a method where at least one of the following is automated: the contacting at a predetermined set of locations; the detecting of abnormal open and short circuits; and the attempting to remove the short circuits (Leedy: column 6, lines 28-58).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the method of Leedy into the method of Lo et al. for the purpose of automatically contacting locations, detecting open circuits and short circuits, and/or

attempting to remove short circuits since it would reduce the possibility of human error or further damage due to additional handling.

Referring to claim 11, Lo et al. discloses a method of automatically testing wiring interconnect packages comprising: contacting a predetermined set of locations on a wiring interconnect package using a cluster probe containing a plurality of probes (claim 1); automatically applying a predetermined set of voltages in a predetermined sequence to predetermined probes in the cluster probe (claim 1); and automatically measuring a response to each application of voltages to detect any short circuits in the wiring interconnect package (claim 1). It should be noted that the processor of Lo et al. controls the whole testing process (column 4, lines 58-61).

Lo et al. does not disclose that open circuits will be detected, or that for any detected short circuits, a predetermined voltage will be automatically applied to attempt to remove the detected short circuits.

Kerschner discloses a method to detect open circuits (column 4, lines 19-39).

Leedy discloses a test and repair method where for any detected short circuits; a predetermined voltage is automatically applied to attempt to remove the detected short circuits (column 6, lines 55-58).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the method of open circuit detection of Kerschner and the repair method of Leedy into the method of Lo et al. for the same purpose as given in claim 9, above.

Referring to claim 12, Lo et al. discloses a relay switching module (fig 1 (42)) for controlling the relays.

Lo et al. does not disclose that the detecting of opens or shorts is executed at a first higher speed using a solid state switching module or that the relay switching module is used to attempt to remove shorts.

Leedy discloses that testing is executed at a first higher speed using a solid state switching module (fig 2 (50)), (column 5, lines 40-42 and 46-48). It should be noted that Leedy uses a computer to analyze data from active device switching circuitry, which could be referred to as a solid state wiring analyzer as shown in claim 2, above. Leedy also discloses an attempt to remove shorts (column 6, lines 60-64).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the solid state switching module and repair method of Leedy into the method of Lo et al. for the purpose of detecting opens or shorts at a higher speed, increasing reliability, reducing the size of components and attempting to remove shorts using relays, since relays are more durable than transistors in that they can handle a larger current or voltage spike used for repairing short circuits.

Referring to claim 13, Lo et al. discloses the method as claimed except for automating the contacting of the wiring interconnect package.

Leedy discloses a method where contacting the wiring interconnect package is additionally automatically actuated by a controller (column 6, lines 28-39).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the method of Leedy into the method of Lo et al. for the purpose

of automatically contacting the wiring interconnect package since it would reduce the possibility of human error or further damage due to additional handling.

Referring to claim 19, Lo et al. discloses a signal-bearing medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus to perform a method of testing wiring interconnect packages (column 4, line 61 – column 5, line 5), comprising: contacting a predetermined set of locations on a wiring interconnect package using a cluster probe containing a plurality of probes (claim 1); applying a predetermined set of voltages in a predetermined sequence to predetermined probes in the cluster probe (claim 1); and measuring a response to each application of voltages to detect any short circuits in the wiring interconnect package (claim 1).

Lo et al. does not disclose that open circuits will be detected, or that for any detected short circuits, a predetermined voltage will be applied to attempt to remove the detected short circuits, where the applying of voltages and measuring of responses to detect any short circuits uses the same apparatus that would be used for attempting to remove the short circuits.

Kerschner discloses a method to detect open circuits (column 4, lines 19-39). Leedy discloses a test and repair method where for any detected short circuits, a predetermined voltage is applied to attempt to remove the detected short circuits (column 6, lines 55-58), where the applying of voltages and measuring of responses to detect any short circuits uses the same apparatus that is used for attempting to remove the short circuits (column 7, lines 10-15).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the method of open circuit detection of Kerschner and the repair method of Leedy into the method of Lo et al. for the same purpose as given in claim 9, above.

New Claims

5. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morrison et al. in view of Leedy (USPN 6,288,561).

Referring to claim 20, Morrison et al. discloses the apparatus as claimed except for a controller to control the said wiring analyzer and to control said current source, wherein said controller controls said wiring analyzer to perform an analysis of all said conductors contacted by said cluster probe prior to attempting to remove any located short circuit and said attempt to remove short circuit occurs without moving said cluster probe.

Leedy discloses a controller (fig. 2 (30)) to control the said wiring analyzer and to control said current source, wherein said controller controls said wiring analyzer to perform an analysis of all said conductors contacted by said cluster probe prior to attempting to remove any located short circuit and said attempt to remove short circuit occurs without moving said cluster probe (column 6, lines 60-64).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Morrison et al. for the purpose of reducing error by providing automatic control and analysis.

Referring to claim 21, Morrison et al. discloses the apparatus as claimed except wherein after attempting to remove said short circuits and prior to moving said cluster probe, said controller thereafter uses said at least one wiring analyzer to again locate shorts between said plurality of conductors.

Leedy discloses the apparatus wherein after attempting to remove said short circuits and prior to moving said cluster probe, said controller thereafter uses said at least one wiring analyzer to again locate shorts between said plurality of conductors. It should be noted that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Morrison et al. for the same purpose as given in claim 20, above.

Referring to claim 22, Leedy discloses the apparatus as claimed except wherein said voltage stress test is executed prior to moving said cluster probe, and prior to moving said cluster probe, said controller uses said at least one wiring analyzer to again locate shorts between said plurality of conductors.

Leedy discloses the apparatus wherein said voltage stress test is executed prior to moving said cluster probe, and prior to moving said cluster probe, said controller uses said at least one wiring analyzer to again locate shorts between said plurality of conductors. It should be noted that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Morrison et al. for the same purpose as given in claim 5, above.

Allowable Subject Matter

6. Claims 2, 8 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed July 10, 2003 have been fully considered but they are not persuasive.

8. In response to Applicant's argument with respect to claims 1 and 14, that "nowhere does Leedy even suggest that any techniques discussed therein could be extended to other arts" (page 10, lines 26-27), it should be noted that as stated in previous office actions as well as in the personal interview, Leedy does disclose the techniques can be extended to other arts (column 3, lines 56-63). Leedy specifically cites other substrates, such as AlN, SiC, quartz, glass or diamond may be tested. Therefore it is clear that even though Leedy discusses the specific details of the invention with respect to processing semiconductor wafers, the invention is also able to handle other substrates, circuit substrate types and substrate assemblies.

9. In response to Applicant's argument with respect to claims 5 and 17, that Leedy does not disclose a high voltage stress test, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Since the controller of Leedy is capable of controlling the voltage between appropriate probe points, it is capable of performing a high voltage stress test.

10. In response to Applicant's argument with respect to the combination of Lo et al. in view of Leedy, it should be realized that nowhere in claims 14-18 is the limitation of "a substrate devoid of components" (page 13, line 15) claimed.

Final Rejection

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J. Dole whose telephone number is 703-305-7396. The examiner can normally be reached on Mon. thru Fri. from 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on 703-308-0750. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TJD

N. Le
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